VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (TWICE AMENDED) An apparatus comprising:

a circuit comprising [one or more] a plurality of inputs configured to provide a selected device identification (ID) from [one of] a plurality of different device IDs, wherein said [one or more] plurality of inputs allow said circuit to be implemented with [said selected one] any of said plurality of different device IDs.

2. (TWICE AMENDED) The apparatus according to claim 1, wherein said selected device [identification] ID comprises a soft code.

4. (TWICE AMENDED) The apparatus according to claim 1, wherein each of said plurality of different device IDs [each provide] identifies a unique configuration of said circuit.

5. (TWICE AMENDED) The apparatus according to claim 1, wherein said selected device identification ID can be [configured] reconfigured after fabrication of said apparatus.

6. (TWICE AMENDED) The apparatus according to claim 1, wherein said circuit comprises:

a logic circuit configured to receive said [one or more] plurality of inputs;

a multiplexer configured to receive an output of said logic circuit; and

a memory element configured to receive an output of said multiplexer.

9. (AMENDED) The apparatus according to claim 1, wherein said [circuit is implemented within] apparatus further comprises a FIFO memory.

10. (AMENDED) The apparatus according to claim 1, wherein said [one or more] plurality of inputs comprise mark options.

11. (AMENDED) The apparatus according to claim 1, wherein said [one or more] plurality of inputs comprise configuration input pins.

13. (TWICE AMENDED) An apparatus comprising:

means for receiving [one or more] a plurality of inputs; and

means for providing a selected device identification (ID) from a plurality of different device IDs, wherein said [one or more] plurality of inputs allow implementation of any of said [selected] plurality of different device [ID] IDs.

14. (TWICE AMENDED) A method for selecting one of a [multiple number] plurality of different device identifications (IDs) comprising the steps of:

(A) receiving [one or more] a plurality of inputs configured to select said one of said plurality of different device IDs; and

(B) [selecting] configuring a device with said selected device identification (ID) [from a plurality of different device IDs], wherein said [one or more] plurality of inputs allow implementation of any of said [selected] plurality of different device [ID] IDs.

15. (TWICE AMENDED) The method according to claim 14, wherein said selected device [identification] ID comprises a soft code.

16. (TWICE AMENDED) The method according to claim 14, wherein each of said different device IDs [each implement] identifies a unique circuit configuration.

17. (AMENDED) The method according to claim 14, wherein said selected device identification ID can be [configured] reconfigured after fabrication.

18. (AMENDED) The method according to claim 14, wherein said [one or more] plurality of inputs comprise mark options.

19. (AMENDED) The method according to claim 14, wherein said [one or more] plurality of inputs comprise configuration input pins.

## REMARKS

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns a circuit comprising a plurality of inputs configured to provide a selected device identification (ID) from a plurality of different device IDs. The plurality of inputs allow the circuit to be implemented with any of the different device IDs (see claim 1 above). Claims 13 and 14 recite similar limitations.

## TELEPHONE INTERVIEW

Applicant's representatives appreciate the kind and courteous discussion held with the Examiner on November 19, 2002. As discussed, the claims have been amended to advance prosecution with respect to the present rejections, particularly based on the IEEE standard 1149.1 identification code/device ID register. The following remarks will further expand on these issues.

## SUPPORT FOR THE AMENDMENTS

Support for the above amendments to the claims can be found in the specification, claims and figures as originally filed. However, by way of example, and without limitation to further support that may be found elsewhere in the original specification, claims and figures, support for the amendments to the claims can be

found as follows (all references to support are to the specification, claims and figures as originally filed):

| Location of Amendment | Support: Specification | Support: Claim(s) | Support: Fig(s). |
|---|---|---|---|
| Claims 1, 6, 10, 11, 13, 14, 18 and 19 | P. 6, ll. 4-8; p. 7, ll. 3-5; p. 7, l. 9-p.8, l. 9 | -- | 2 |
| Claim 4 | P. 5, ll. 5-8; p. 9, l. 16-p. 10, l. 2 | -- | -- |
| Claim 9 | P. 4, ll. 18-19; p. 7, l. 17-p. 8, l. 7 | -- | 3 |

Thus, no new matter is introduced by the present amendment.

## CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-4, 6-16, and 18-20 under 35 U.S.C. §102(b) as being anticipated by the background section of the present application and/or FIG. 1 of the present application is traversed.

At no point in the background section of the present application is there disclosed or described a circuit having a plurality of inputs configured to provide a selected device ID from a plurality of different device IDs, wherein the plurality of inputs allow the circuit to be implemented with any of the different device IDs, as is presently claimed.

For example, the circuit of FIG. 1 of the present application has exactly zero (0) inputs configured to provide a selected device identification. The present specification states that "hard coded logic block 12 is implemented to provide the device ID." (Page 3, line 2 of the present specification.) FIG. 1 of the present application shows exactly zero (0) inputs into logic block 12.

Therefore, FIG. 1 of the present application cannot disclose a circuit having a plurality of inputs configured to provide a selected device ID from a plurality of different device IDs, as recited in the present claim 1. Thus, FIG. 1 of the present application cannot disclose all of the elements recited in the present claim 1. As a result, FIG. 1 of the present application cannot anticipate the present claims 1-4 and 6-12.

The background section of the present application describes the logic block 12 in FIG. 1 as using a metal option or bond options (page 3, lines 3-4 of the present specification). However, metal options and bond options are simply hard-wired connections between two nodes, which cannot be changed after device fabrication (see, e.g., page 3, lines 3-5 of the present specification). Furthermore, as stated at page 2, lines 4-5 of the present specification, the logic circuit 12 is configured to present either a '1' or a '0' to the multiplexer 14 and cannot be changed.

One of ordinary skill in the art would understand these statements from the background section to mean that the metal option or bond options in logic circuit 12 are hard-wired connections to nodes configured to be at a certain logic level ("1" or "0") at all times (e.g., a power supply such as Vcc or ground). A hard-wired connection to such a node cannot provide a selected device ID from a plurality of different device IDs or allow the circuit to be implemented with any of the plurality of different device IDs, as recited in the present claim 1 (emphasis added).

Therefore, the description of the circuit of FIG. 1 in the background section of the present application does not disclose a circuit having a plurality of inputs (i) configured to provide a selected device ID from a plurality of different device IDs or (ii) that allow the circuit to be implemented with any of the plurality of different device IDs, as recited in the present claim 1. Thus, the description of the circuit of FIG. 1 in the background section of the present application does not disclose all of the elements recited in the present claim 1. As a result, the description of the circuit of FIG. 1 in the background section of the present application does not anticipate the present claims 1-4 and 6-12 and the rejection should be withdrawn.

Finally, the description of the optional 32-bit ID code/device ID register in the IEEE 1149.1 standard on page 1 of the present application (hereinafter "Applicant's IEEE 1149.1

register description") does not anticipate the present claims. As is well known in the art, a single register generally has only a single data line in (see, e.g., col. 4, lines 43-45, col. 6, line 63-col. 7, line 19, col. 12, line 52-col. 13, line 12, and FIGS. 3, 6 and 10 of Carmichael et al. '311, and col. 2, ll. 35-59 of Swoboda et al. '824, both cited against the present claims 5 and 17). Consequently, Applicant's IEEE 1149.1 register description would be understood by one skilled in the art to have only a single input providing device ID code information.

Therefore, Applicant's IEEE 1149.1 register description does not disclose or describe a circuit having a plurality of inputs configured to provide a selected device ID from a plurality of different device IDs, as recited in the present claim 1. Thus, Applicant's IEEE 1149.1 register description does not disclose all of the elements recited in the present claim 1. As a result, no part or parts of the background section of the present application anticipate(s) the present claims 1-4 and 6-12.

Similarly, the present claim 13 recites means for receiving a plurality of inputs and means for providing a selected device identification (ID) from a plurality of different device IDs, wherein the plurality of inputs allow implementation of any of the plurality of different device IDs. The present claim 14 recites receiving a plurality of inputs configured to select one of the plurality of different device IDs wherein the plurality of

inputs allow implementation of any of the plurality of different device IDs. The background section of the present application does not disclose or suggest these elements. Accordingly, claims 13 and 14 are fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 5 and 17 under 35 U.S.C. §103(a) as being obvious over the background section of the present application, in view of Swoboda et al. '824 or Carmichael et al. '311 is respectfully traversed and should be withdrawn. Claims 5 and 17 depend from independent claims 1 and 14, which are now believed to be allowable.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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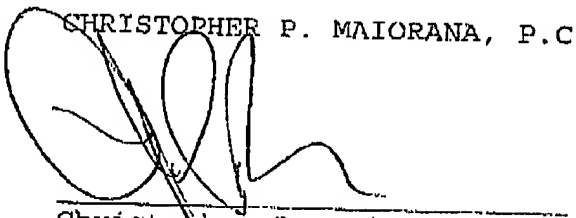

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